Semiconductors Run the World

Hot Chips 2022
Pat Gelsinger, Intel CEO
Final Program
Monday, August 14, 1995—Memorial Auditorium

9:30–9:15 Welcome and Opening Remarks
Nam Ling, General Chair
Hasan B. Ahmedi and Norman P. Jouppi, Program Co-Chairs

9:15–10:45 Session 1: Embedded Processors
Session Chair: Robert Garner, Sun Microsystems

1.1 The First Superscalar 29K™ Family Member
B. McMillin, Advanced Micro Devices
1

1.2 The Architecture of the NS486 Integrated Processor
M. D. Namirovsky, National Semiconductor
11

1.3 The MinIRISC™ CW4010: A Superscalar MIPS Processor ASIC Core
P. Cobb, J. Cea, LSI Logic
19

10:45–11:15 Break

11:15–12:15 Keynote Address: “Nanometers and Gigabucks”
Gordon Moore, Chairman of Intel Corporation

12:15–1:45 Lunch

1:45–3:15 Session 2: x86 Processors
Session Chair: Mark Horowitz, Stanford University

2.1 Optimizing the P6 Pipeline, D. Papworth, Intel Corporation
31

2.2 AMD-K8™ Microprocessor
D. Christie, Advanced Micro Devices
41

2.3 Building a Better Beast: Native vs. RISC-like vs. VLIW
T. Darby, Cyrix
49

3:15–3:45 Break

3:45–5:15 Session 3: RISC-1
Session Chair: Winfried W. Wielick, Hal Computer Systems

3.1 Performance Evaluation of the Superscalar Speculative Execution Hal SPARC64 Processor
S. Aizen, S. Goldstein, Hal Computer Systems
59

3.2 SPARC64™: HAL’s Second Generation 64-bit SPARC Processor
G. W. Shen, Hal Computer Systems
75

3.3 Memory Performance Features of the 64-bit PA-6000
S. Nuss, Hewlett-Packard
87

5:15–7:00 Monday Evening Buffet Dinner

7:00–9:00 Evening Panel Session: What is the Role of Competing Architectures in an x86 World Order?
Moderator: John Wharton, Consultant/Analyst, Applications Research. Panel members: Keith Diefendorf, Senior Member Technical Staff, Motorola; Davit Dzitaz, President and CEO, Transmeta Corporation; John Novakley, Director, CPU Products Group, MicroModule Systems; Nick Trivedi, CFO, Technos International; Pace Wallon, Director, Microsystems Architecture, Groupe Bull
CHIPS for America Act

“Since semiconductors are such key components, the fragile supply chain for semiconductors puts virtually every sector of the economy at risk of disruption.”

- Department of Commerce’s E.O. 14017 industrial base review
Tech Superpowers

Ubiquitous

Compute × Connect × Infrastructure × Artificial Intelligence
Systems Foundry

- Wafers
- Packaging
- Chiplets
- Software

intel

Open Source
Moore’s Law Alive and Well

Future projections based on products still in design. Future transistor counts are projections and are inherently uncertain.
We will not rest until the periodic table is exhausted
“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”

- Gordon E. Moore

1. “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965
Intel Package Technology

**Package main function:** provide power and signaling from motherboard to die

**Added Package value:** high density interconnects that enable larger die complexes from multiple process nodes

*Graphic is for illustrative purposes only and is not to scale*
Open Chiplet: Platform on a Package

- 20X I/O Performance at 1/20th Power* relative to PCIe G5 x16

* relative to PCIe G5 x16

White Paper: Universal Chiplet Interconnect Express (UCle®): Building an open chiplet ecosystem, Dr. Debendra Das Sharma, Intel Senior Fellow and Chief Architect, I/O Technologies and Standards Promoter Member of UCIe
“Software is the soul of the machine.”

-Greg Lavender
In Summary

- Silicon design remains essential – HW/SW co-design is critical
- The action is in the edges (Mobile & Server)
- Cloud becomes the Software-Defined Datacenter
- Big Data opens up new opportunities for HW design
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**IFS as an Open System Foundry**

- **System Software**: x86, arm, RISC-V, Intel® Simics
- **System of Chips**: System Partitioning, Intel® Chiplet Studio™ Suite
- **Accelerated Silicon Services**: Intel® Docea™, Intel® Cofluent™
- **Package & Interconnect Optimization**: Intel Chiplet Interconnect Express (UCle), EMIB, Foveros
- **Silicon**: Intel 16, Intel 3, Intel 18A

**Features**:
- Security – Manageability – Test/Debug
- Differentiated IP
- Architecture
- Thermals
- Performance
- Validation
- Universal Chiplet Interconnect Express (UCle)
- EMIB
- Foveros
Stewards of Moore’s Law
In the Golden Age of Semiconductors