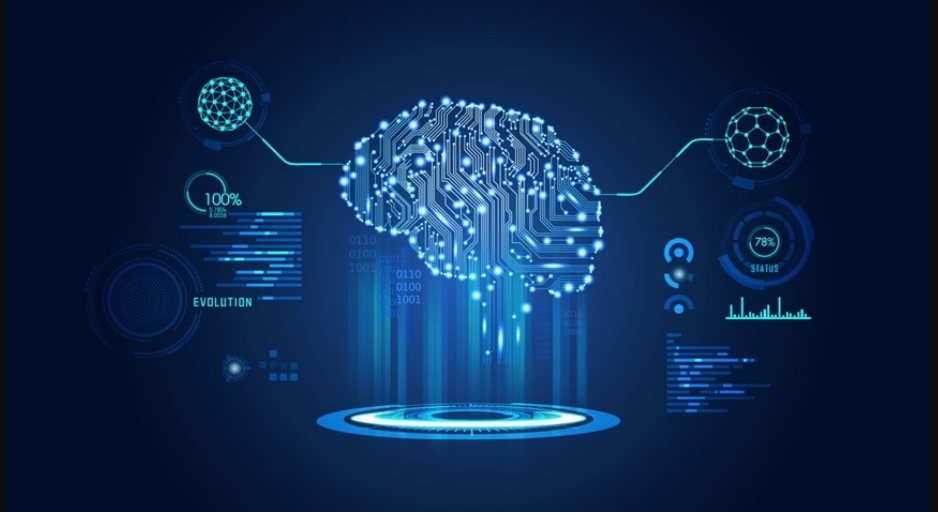

Enabling Scalable Application-Specific Optical Engines (ASOE) by Monolithic Integration of Photonics and Electronics

Christoph Schulien, HotChips 2022, August 22, 2022

RANOVUS™

Acknowledgements

I'd like to emphasize that the development of the ODIN® technology is based on the contributions of the entire team at Ranovus

Without each individual's contributions this achievement would have not been possible.

Outline

- Key Drivers for Optical Interconnect
- Ranovus Monolithic Platform ODIN®
  - Applications Space and Design Targets
  - System Design Approach
  - Enabling Technology
- Monolithic EPIC Design and Key Building Blocks
  - 100G PAM-4 Ring Resonator Modulators (RRM)
  - 100G PAM-4 RF Electronics
  - Fiber Assembly, Lasers, Packaging
- ODIN®8P Test Results
- Summary & Outlook

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Key Drivers for Optical Interconnect

AI/ML Workloads Require more & more Compute & Memory

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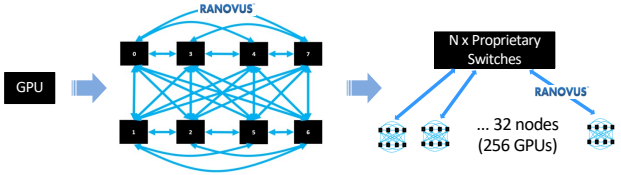
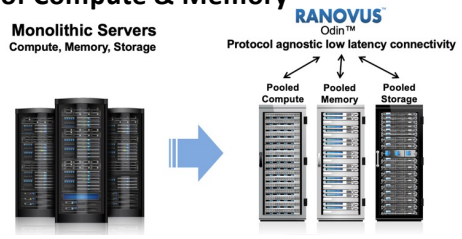
- **GPU & ML ASIC Scale out**

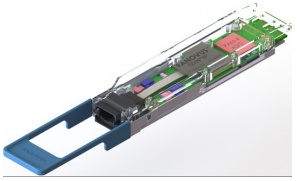


- **Disaggregation of Compute & Memory**



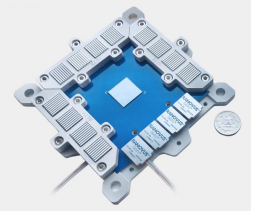
- **Ethernet Switching Networks**

Application Specific Optical Engines



Pluggable Module

Near Packaged Optics



Co-Packaged Optics

What does it take to build **A**pplication **S**pecific **O**ptical **E**ngines (ASOE) ?

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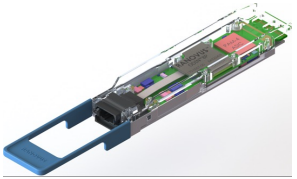
- Knowledge of the Application & Systems
- Complete End to End System Model
- Differentiated and Validated IP in:
  - High-Speed Mixed-Signal Electronics
  - Silicon Photonics (SiP)
  - Lasers
  - Advanced Packaging
  - Advanced Manufacturing & Testing
- Differentiated Foundries for Electronics/SiP/Laser chips
- Differentiated OSATs for Manufacturing and Testing

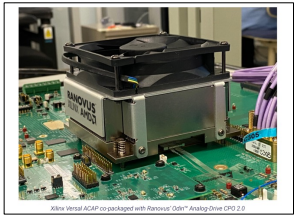
Miniaturization is the Key Design Target to Meet Performance, Cost, Power & Latency Requirements

Application Specific Optical Engines

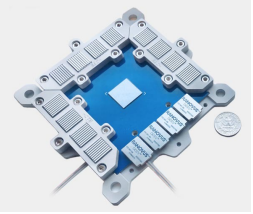


Pluggable Module

Near Packaged Optics



Xilinx Versal ACAP co-packaged with Ranovus' Odin™ Analog-Drive CPO 2.0



Co-Packaged Optics

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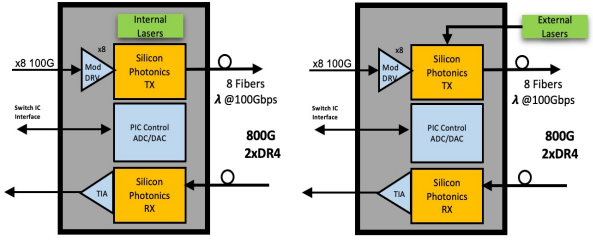
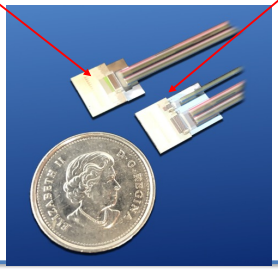
ODIN®8P EPIC Design Objectives

Two Initial Variants for Different Target Applications



ILS Version
(ILS: **I**ntegrated **L**aser **S**ource)

ELS Version
(ELS: **E**xternal **L**aser **S**ource)



EPIC: Electronic/Photonic IC

- **Monolithically integrated fully bidirectional 800G analog optoelectronic (O/E) engines on a single EPIC die – protocol agnostic**
- **Target applications:**
  - **Co-Packaged Optics (CPO) chiplets for integration with large Switch ASIC or CPU/GPU (typically an ELS use case)**
  - **Integration with close proximity PAM4 DSP in pluggable modules for Ethernet applications (typically an ILS use case)**
- **Full compliance to Ethernet DR-4+ specifications, including full interoperability**
- **Power dissipation target: < 4W**
- **Enabling further power savings when operated in an optimized proprietary link (e.g. by lowered laser power)**
- **These versions are first instantiations of a series of chips for the ODIN® Application-Specific Optical Engine (ASOE) product family**

End to End System Design for Analog OE

A Specific Challenge for Direct-Drive Optics

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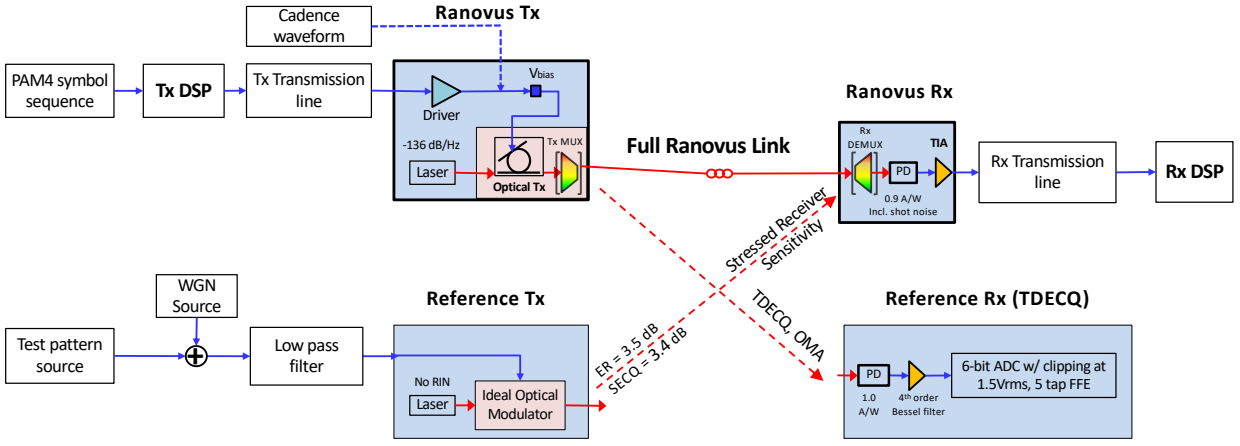
The challenge:

- **An analog or direct-drive optical engine (OE) is representing only the analog front-end part of a complete transmission channel**
- **Transmission end points are determined by the Tx and Rx of the respective SerDes employed**
- **For high symbol rates and/or longer electrical interconnects, overall system performance equally depends on SerDes analog features and equalizer capabilities as well as on OE features**
- **SerDes is always a third-party element**
  → close cooperation required with partners owning the SerDes IP

Typical co-design scenario:

- **Ranovus and SerDes partner share models for their respective elements on a chosen platform:**
  - IBIS-AMI is one option, running on a system/signal integrity simulator (e.g.: Keysight ADS)
  - Other option: directly sharing Matlab models
  - Owner of the board/package design provides s-parameters to describe the electrical interconnects – typically gained from 3D EM simulations

Ranovus Custom OE Transmission Model



SECQ: Stressed Eye Closure, Quaternary
ER: Extinction Ratio

TDECQ: Transmitter & Dispersion Eye Closure, Quaternary
OMA: Optical Modulation Amplitude

System Simulation Setup for Interworking (against Reference Tx / Rx) or for End-End Link Modeling

IBIS-AMI Optical Re-Driver Model

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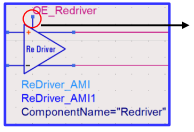
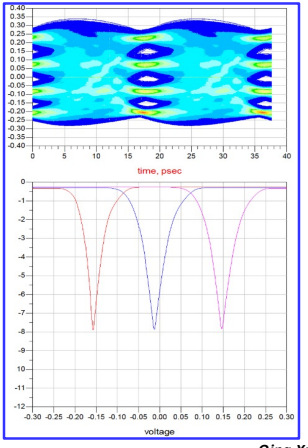
Compiled version of Matlab model

- Purpose: Co-simulation of complete electrical-optical-electrical (EOE) chain with packaged Serdes model and s-parameters
- EOE re-driver model variables
  - RRM Detuning Frequency (Hz)
  - Channel Loss (dB)
  - LaserPower
  - Gain (dB)
  - Configuration
  - Modulation
  - ModType
  - DesignType
  - DRVType
  - bePlot
  - Debug



Re-Driver symbol for ADS simulator

Example: output waveform from IBIS-AMI simulation with Re-Driver model



Qing Xu et al.,

End-to-end IBIS-AMI Modeling and Simulations of Electrical/Optical Links

Technology Platform for Monolithic EPIC SOC Integration

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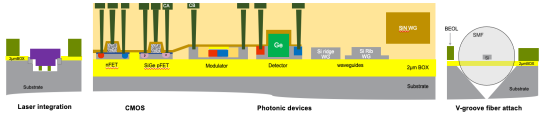
GF 45SPCLO SiPh Foundry Offering
Technology Overview

- High performance photonic passive and actives device library
- Monolithic integration of high performance 45nm RF SOI CMOS
- Dual SOI thickness: 160nm photonics, 88nm CMOS; 2µm BOX, SOI and SiN waveguides
- State-of art 300mm Fab8 Malta Fab, leveraging advanced immersion lithography
- Freeform design enabled with curve-linear GDS with advanced OPC
- Passive v-groove fiber array / attach, 250µm, 127µm pitch
- State-of-Art PDK enablement with EO co-design environment, standard cell digital library
- Automated electrical / optical wafer level test



Global Foundries material courtesy of Vikas Gupta

Beside using foundry PDK, Ranovus owns or co-develops critical IP:

- **R**ing **R**esonator **M**odulator (RRM)
- Lasers & laser attach design / process
- Fiber assembly process
- All electronic designs, including RF building blocks and control IP

Ranovus chose Global Foundries' 45nm Process 45SPCLO as the optimum EPIC integration platform

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ODIN®8P EPIC, ELS Version – Key Functional Blocks

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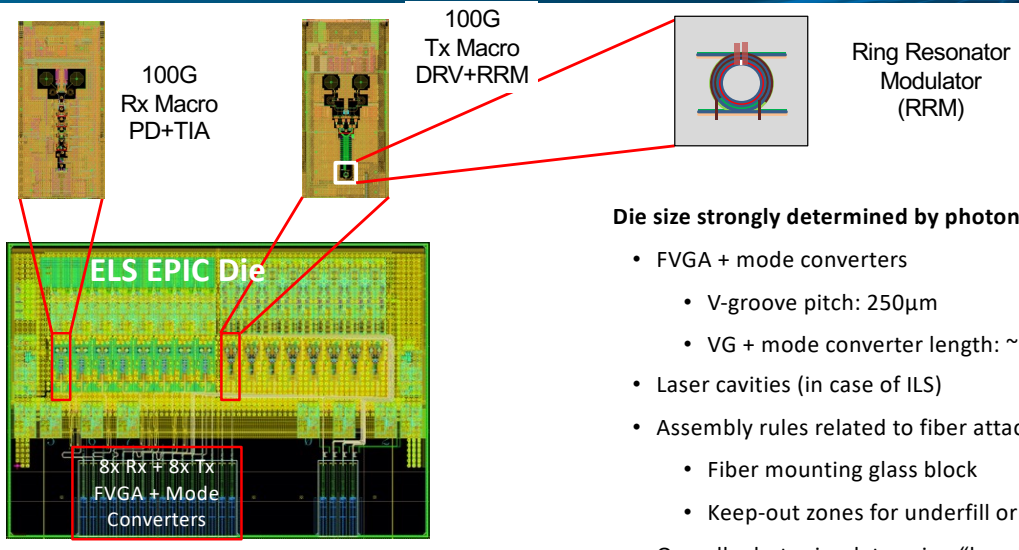
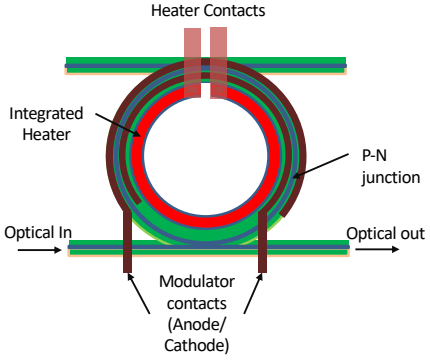


Die size strongly determined by photonics:

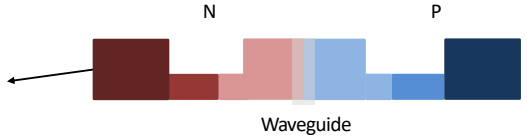
- FVGA + mode converters
  - V-groove pitch: 250µm
  - VG + mode converter length: ~2mm
- Laser cavities (in case of ILS)
- Assembly rules related to fiber attach, for things like:
  - Fiber mounting glass block
  - Keep-out zones for underfill or epoxy outflow etc.
- Overall: photonics determine “beachfront” width

Ring Resonator Modulator (RRM) Design

RRM are key enablers for very compact optical transmitters, because of their small footprint (typically < 50x50 µm²)

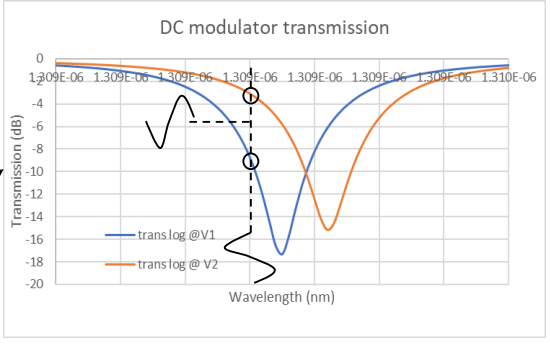


Modulate charge carrier concentration in reverse-biased pn junction



Modulate resonance wavelength

Modulate transmitted amplitude of single-λ input



System Simulation Input: Proprietary Dynamic Nonlinear RRM Time Domain Model

100G Tx Macro (DRV+RRM)

Design Requirements & Extracted Simulation Results

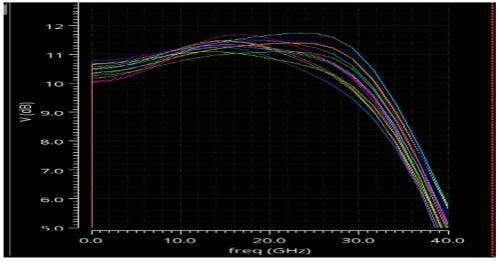
RANOVUS™

Single-stage fixed gain linear RRM driver:

- **Differential Drive Stacked Cascodes**
- **On-chip AC coupling**
- **3dB BW:** **>35GHz**
- **RF gain:** **>10dB**
- **Low freq. corner:** **<50kHz**
- **Min. linear output voltage:** **>2$V_{diff,pk-pk}$**
- **Single supply:** **3.3V**
- **Power dissipation:** **<100mW**

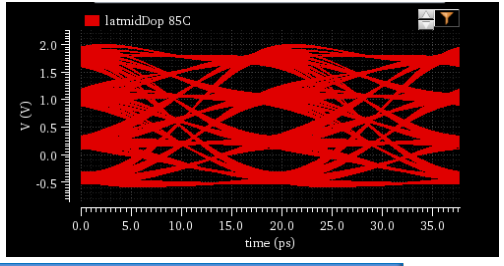
Driver AC magnitude response:

- **Voltage gain vs. frequency**
- **Input Port → RRM junction**
- **Corner simulations (PVT)**



Driver Transient Response:

- **Drive voltage @RRM junction**
- **Ideal input PRQS waveform**
- **Typical corner, @ 85 °C**



System Simulation Input: Time Domain Waveforms or Frequency Responses

100G Rx Macro (PD+TIA)

Design Requirements & Extracted Simulation Results

RANOVUS™

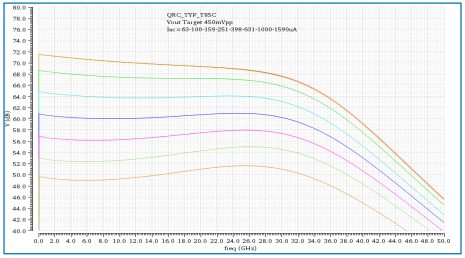
PD: Photodetector; TIA: Transimpedance Amplifier

Multistage O/E Converter Amplifier :

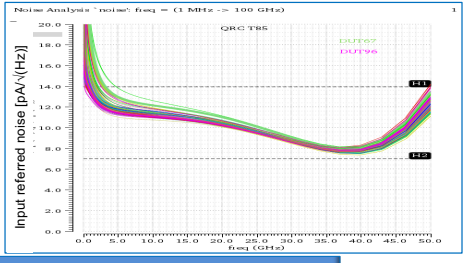
- **TIA + SE/Diff + 3xVGA + Buffer**
- **3dB BW:** **>30GHz**
- **TIA max gain:** **~72dBΩ (4kΩ)**
- **Low freq. corner:** **<50kHz**
- **Output Swing Target:** **450mV$_{diff,pk-pk}$**
- **Input referred noise:** **<14pA/√(Hz)**
- **Performance PVT-stabilized**

- **Single supply:** **1.8V**
- **Power dissipation:** **<120mW**

Typical AC Magnitude Response over Gain Setting @ 85 °C



Input Referred Noise Spectrum, Monte Carlo Simulation @ 85 °C / max gain

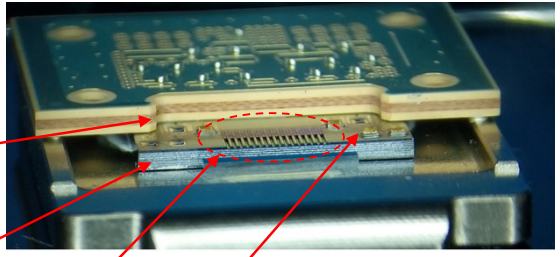


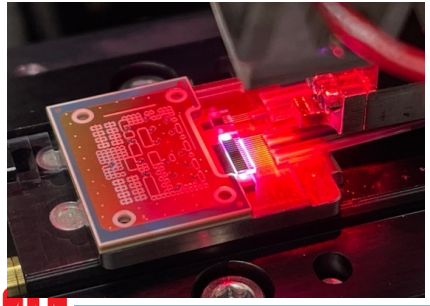
System Simulation Input: Time Domain Waveforms or Frequency Responses
(e.g. magnitude, phase + noise current spectral density)

ODIN® EPIC Fiber Attach & Packaging

16 Fiber passive V-Groove attach system

- Flip-chip technology used for SiP with V-Groove
- Passive attach of 16 fiber array
- Performance Targets:
  Insertion Loss <2dB per facet/connection - across complete 16 channel fiber array
- Reliability:
  Telcordia Damp Heat, High-Temperature Storage & Temperature Cycling





EPIC on fiber assembly station

EPIC variants with fiber array attached to FVGA

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Traffic Test Setup for ODIN®8P OE

Demonstrated with Xilinx at OFC 2022

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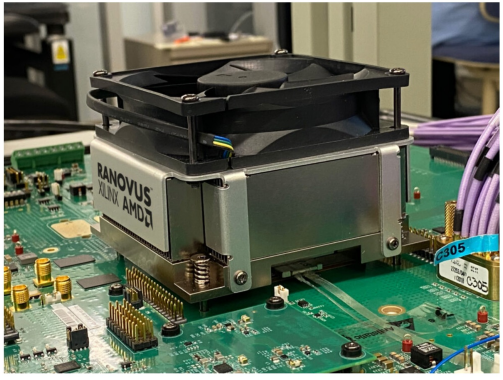
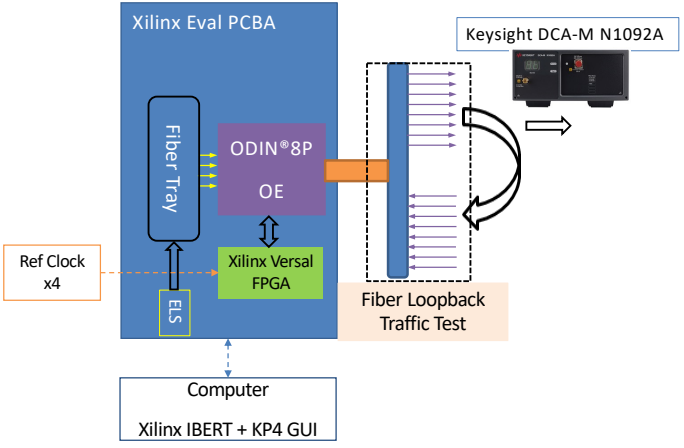
Xilinx Eval PCBA hosting
Versal™ FPGA co-packaged with ODIN®8P OE

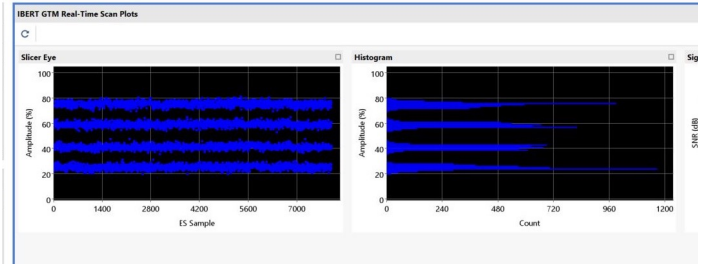


Xilinx Versal ACAP co-packaged with Ranovus' Odin™ Analog-Drive CPO 2.0

Block Diagram of Traffic Test Setup



106.25Gbps PAM4 Fiber Loopback BER



100G PAM4 - Slicer Eye & Histogram Sample

Link Group 0 (8)		Reset	Reset	Reset				BER	PRBS 31	PRBS 31
Link 0	IBERT_0.Quad_206.CH_2.TX IBERT_0.Quad_206.CH_2.RX	Reset	Reset	Reset	106.219 Gbps	4.359E12	5.773E5	1.275E-7	PRBS 31	PRBS 31
Link 1	IBERT_0.Quad_206.CH_0.TX IBERT_0.Quad_206.CH_0.RX	Reset	Reset	Reset	106.219 Gbps	4.301E12	5.68E4	1.283E-8	PRBS 31	PRBS 31
Link 2	IBERT_0.Quad_205.CH_2.TX IBERT_0.Quad_205.CH_2.RX	Reset	Reset	Reset	106.242 Gbps	4.273E12	2.497E5	5.753E-8	PRBS 31	PRBS 31
Link 3	IBERT_0.Quad_205.CH_0.TX IBERT_0.Quad_205.CH_0.RX	Reset	Reset	Reset	106.219 Gbps	4.125E12	1.272E4	3.004E-9	PRBS 31	PRBS 31
Link 4	IBERT_0.Quad_204.CH_2.TX IBERT_0.Quad_204.CH_2.RX	Reset	Reset	Reset	106.219 Gbps	4.02E12	2.301E5	5.731E-8	PRBS 31	PRBS 31
Link 5	IBERT_0.Quad_204.CH_0.TX IBERT_0.Quad_204.CH_0.RX	Reset	Reset	Reset	106.219 Gbps	3.922E12	2.73E4	6.847E-9	PRBS 31	PRBS 31
Link 6	IBERT_0.Quad_203.CH_2.TX IBERT_0.Quad_203.CH_2.RX	Reset	Reset	Reset	106.219 Gbps	3.686E12	1.153E5	3.073E-8	PRBS 31	PRBS 31
Link 7	IBERT_0.Quad_203.CH_0.TX IBERT_0.Quad_203.CH_0.RX	Reset	Reset	Reset	106.242 Gbps	3.688E12	6.131E4	1.669E-8	PRBS 31	PRBS 31

100G PAM4
8 channels BER results

BER below ~1E-7 for all channels (>3 decades of margin vs. IEEE spec)

106.25Gbps PAM4 TX Quality

Averaged Optical Tx from ODIN®8P

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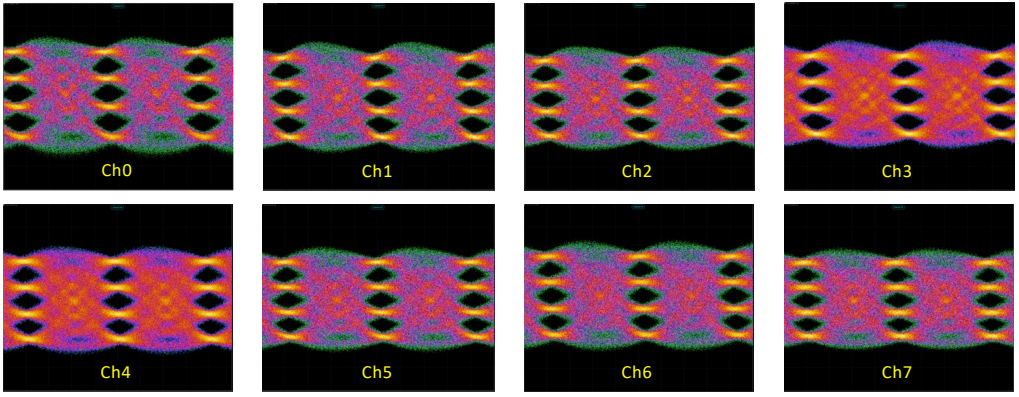
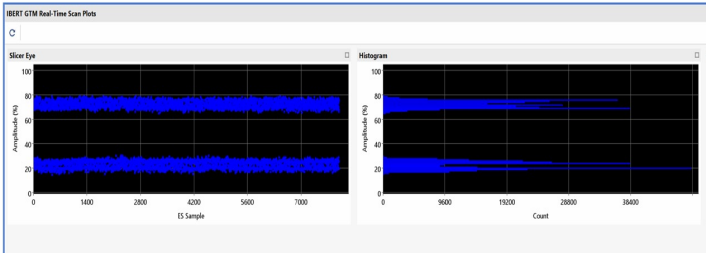


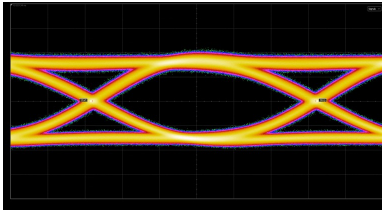
Channel		Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
TDECQ (dB)	After IEEE 802.3bs TDECQ EQ	1.29	1.19	1.00	1.09	1.30	1.57	1.39	1.56

Optical Tx passing IEEE 802.3bs TDECQ spec (< 3.5dB) with good margin

Error-free 32Gbps NRZ Operation



32G NRZ – Slicer Eye & Histogram Sample



32G NRZ
Eye Diagram Sample
@Rx Output

ODIN® is protocol & data rate agnostic – ready to support PCIe Gen5 application

ODIN®8P 800G EPIC Power Consumption

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Power consumption as measured on multiple units, design targets achieved or exceeded

	ELS Version		ILS version	
Element	**Consumption [W]**	**Efficiency [pJ/bit]**	**Consumption [W]**	**Efficiency [pJ/bit]**
Lasers	N/A		1.2 – 1.5	
Tx RF Channels	0.7 – 0.8		0.7 – 0.8	
Rx RF Channels	1.0 – 1.1		1.0 – 1.1	
Other circuitry	0.5 – 0.6		0.5 – 0.6	
Total	**2.2 – 2.5**	**2.75 – 3.1**	**3.4 – 4.0**	**4.25 – 5.0**

ODIN®8P enabling lowest power 2x400GE-DR4 QSFP/OSFP module designs

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- Key Drivers for Optical Interconnect
- Ranovus Monolithic Platform ODIN®
  - Applications Space and Design Targets
  - System Design Approach
  - Enabling Technology
- Monolithic EPIC Design and Key Building Blocks
  - 100G PAM-4 Ring Resonator Modulators (RRM)
  - 100G PAM-4 RF Electronics
  - Fiber Assembly, Lasers, Packaging
- ODIN®8P Test Results
- Summary & Outlook

It takes a lot to build
Application **S**pecific **O**ptical **E**ngines (ASOE) !

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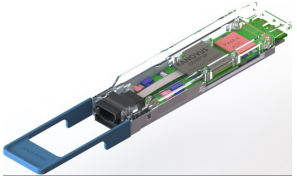
- Knowledge of the Application & Systems
- Complete End to End System Model
- Differentiated and Validated IP in:
  - High-Speed Mixed-Signal Electronics
  - Silicon Photonics (SiP)
  - Lasers
  - Advanced Packaging
  - Advanced Manufacturing & Testing
- Differentiated Foundries for Electronics/SiP/Laser chips
- Differentiated OSATs for Manufacturing and Testing

Miniaturization is the Key Design Target to Meet Performance, Cost, Power & Latency Requirements

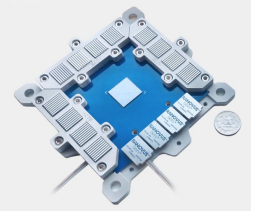
Application Specific Optical Engines



Pluggable Module

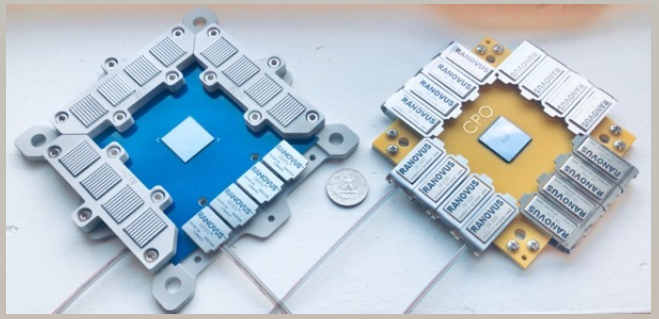
Near Packaged Optics

Xilinx Versal ACAP co-packaged with Ranovus' Odin™ Analog-Drive CPO 2.0



Co-Packaged Optics

Thank You!



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Multi Terabit platform for optical interconnect

Backup Slides

Typical System Design Workflow – IBIS-AMI

(Joined Development with SerDes Partner)

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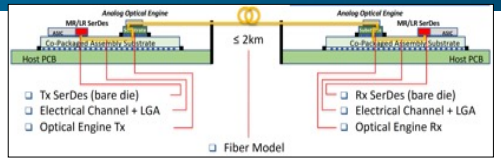

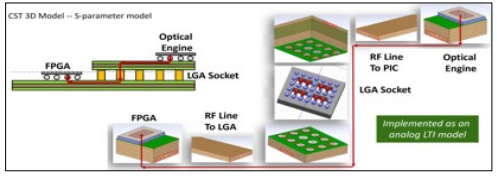

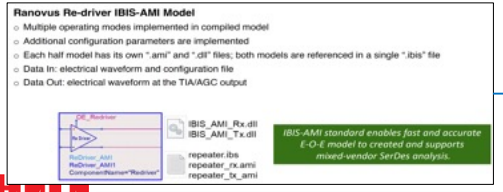

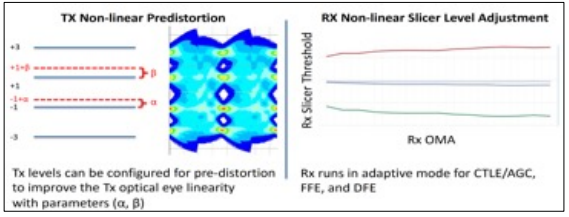

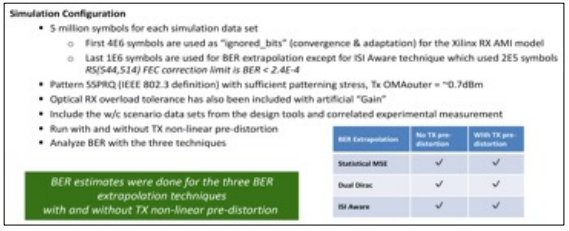

Joint work between Xilinx & Ranovus, presented @ DesignCon 2021

Received Best Paper Awarded

Monolithic EPIC Integration

Implications, Benefits & Challenges

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Some Implications:

- **Photonics implemented by planar waveguides (WG) in Si**
- **To provide optical confinement, waveguides must be embedded in a lower index material (SiO_2)**
  - WG & active circuits constructed above a thick buried oxide (BOX), constituting an SOI technology
- **Different properties for TE and TM WG modes:**
  → Polarization management becoming increasingly important

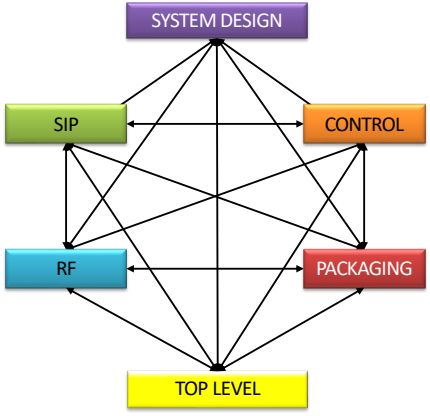
Benefits:

- **Enables a true opto-electronic system-on-chip**
  - Smallest possible size of a solution, as all functional blocks are on single die
  - Simplified packaging (no complex die-on-die etc.)
- **Super low-parasitic RF interconnect between photonic (modulator, Photodetector – PD) and RF elements (modulator driver – DRV, transimpedance amplifier - TIA)**
  - No impedance matching required
  - Enables best-in-class power dissipation
  - Enables superior TIA noise performance
- **SOI prevents substrate coupling and X-talk**

Challenges:

- **BOX related thermal limitations need to be taken into account in circuit design**
- **No metal allowed in close vicinity of optical waveguides**
  - **R**outing constrained, as only upper metal layers can be used to cross WG
- **Narrow Si WG have non-negligible insertion loss, should be kept as short as possible**
  - **P**lacement & routing constrained
- **Optical I/O (i.e. interfacing to optical fiber) requires significant space**
  - For **F**iber **V**-**G**roove **A**rrays (FVGA) and mode conversion

EPIC Design & Integration



Design challenges for a monolithic EPIC SOC :

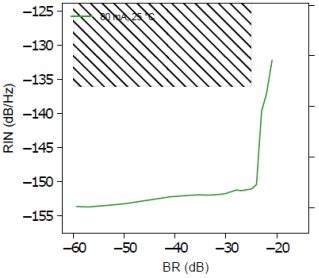
- Interactive multidisciplinary workflow required
- Strong interdependencies make floor planning and integration a highly iterative process
- Packaging & assembly requirements also need to be considered in floor planning

O-Band Lasers for EPIC Integration

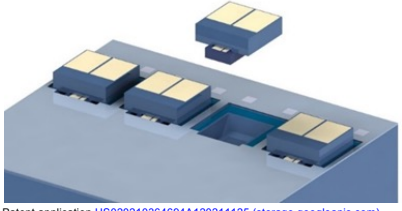
ILS concept

- **ODIN® DFB O-Band Laser**
  - **Co-Designed to support SiP Optical/Physical Interface**
  - **Optical**
    - Designed for back-reflection (BR) resilience
      - Isolator free interface
    - RIN (Relative Intensity Noise) performance under BR
    - Power/Size Efficiency
  - **Physical**
    - Size minimized for EPIC mounting
    - Customized for precise passive mounting

ILS Back-reflection Resilience – RIN vs. BR



- **Innovative laser mounting mechanism, supporting**
  - **Mounted/soldered laser and test before attach**
    - Relaxed tolerances for submount attach
  - **Burn in capability before attach**
  - **Features and facility to perform machine vision/optical alignment**



Patent application US020210364694A120211125 (storage.googleapis.com)