HOTCHIPS 2022

Heterogenous Integration Enables FPGA Based Hardware Acceleration for RF Applications

Sergey Shumarayev

Allen Chan

Tim Hoang

Programmable Solution Group (PSG) CTO Office

Robert Keller

Texas Instruments

This work is supported by the DARPA MTO office
[DARPA CHIPS Contract Number: HR00111830002]

Outlines

- 5G Use Cases and Massive MIMO Typical Base Station
- Motivation
- DARPA CHIPS Program
- Building Blocks
- Growing AIB-Based Chiplet Portfolio
- Chiplet Connection with EMIB and AIB
- Chiplet Integration
- AFE Chiplet Design Features
- Heterogeneous Integration Advantages
- CHIPS Phase 2 Platform Hardware Overview
- Enabling Massive MIMO
- Enabling Radar System
- Enabling Next Generation Systems
- Conclusion

5G Use Cases and Massive MIMO Base Station

5G Use Cases

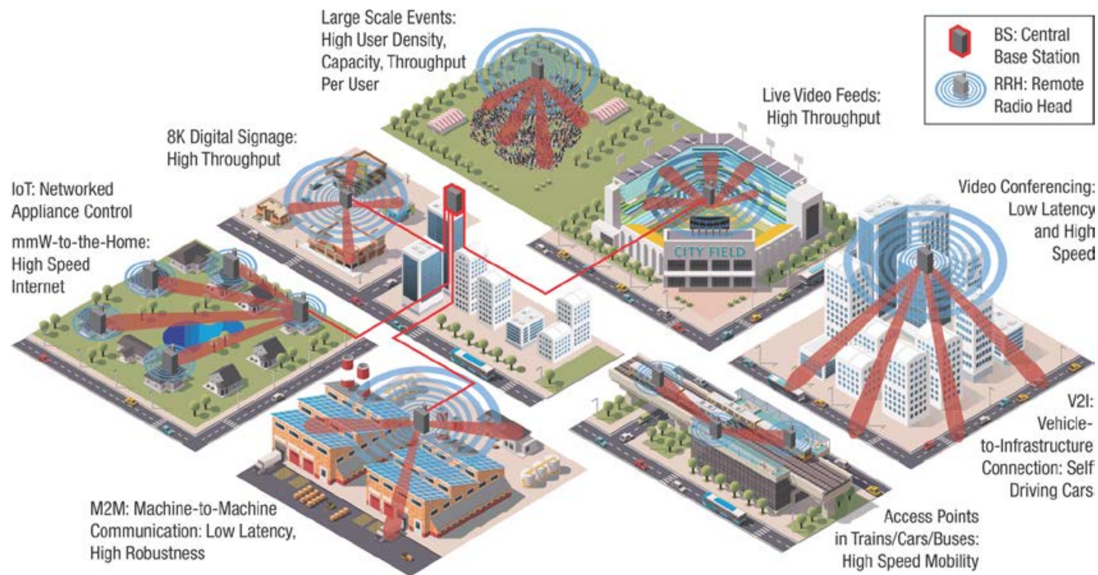
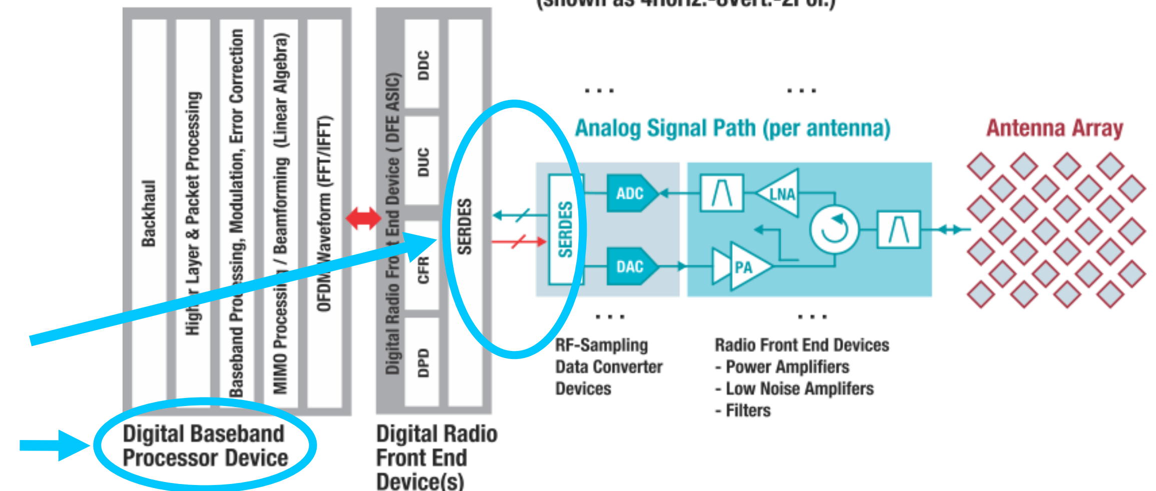


Diagram of typical base station with massive MIMO channels

	JESD 204B
BW	308Gbps
Channels	26 @ 12.5Gbsp
Power	25W
Latency	135 Frame Clk
Board Complexity	High

Bandwidth/Power?

Workload execution time?



Motivation

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."

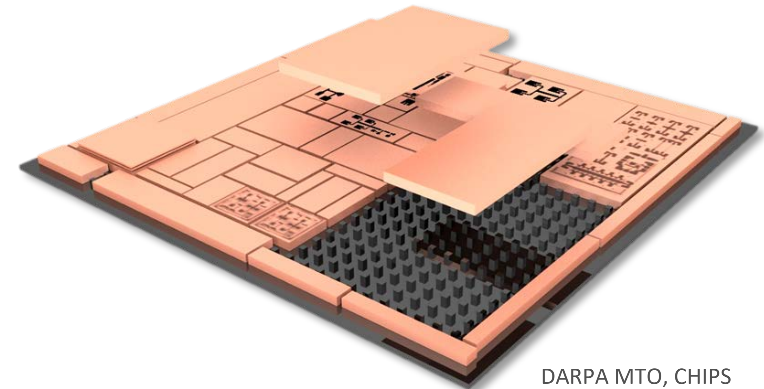
—Gordon E. Moore
Moore's Law paper

DARPA CHIPS Program

CHIPS program seeks to establish a new paradigm in IP reuse. The vision of CHIPS is an ecosystem of discrete modular, reusable IP blocks, which can be assembled into a system using existing and emerging integration technologies.

Successful assembly of chiplets of various sizes into a heterogeneously integrated system resulting in:

- Shorter design development
- Lower-risk design integration
- Lower-cost design implementation
- System power reduction
- Board area complexity reduction
- Board design simplification



DARPA MTO, CHIPS

Chiplets as Building Blocks

- Using chiplets from different process nodes and foundries (including GF, TSMC and Intel) as building blocks to create more complex systems demonstrates effectiveness of heterogeneous integration
- Employing Advanced Interface Bus (AIB) and Intel EMIB technology, chiplet concept was successfully demonstrated in CHIPS Phase 1 with 64 Gsps data converters
- In CHIPS Phase 2, chiplet concept is proven for repeatability with a TI analog front end (AFE) with up to 16TX16RX4FB at 12Gsps and 4Gsps for DAC and ADC respectively
- AIB Public Specification and Hardware Open Source available to download via Github

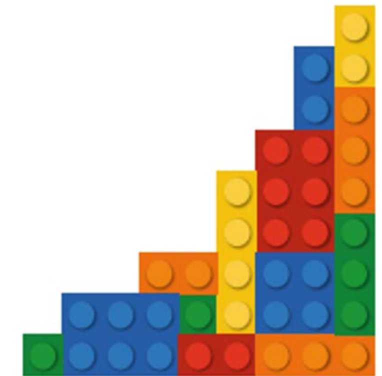
See datasheet for workloads and configurations. Results may vary.

intel.

Advanced Interface Bus (AIB) Specification

2019.9.18
Revision 1.2

At https://github.com/chipsalliance/aib-phy-hardware



Growing AIB-Based Chiplet Portfolio

Technology & Foundry Agnostic

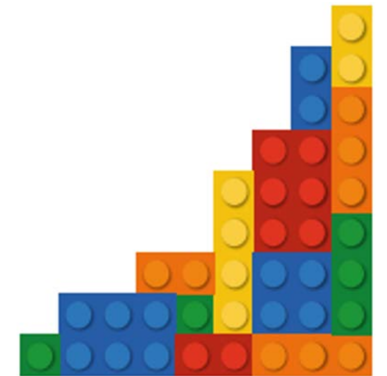
- 2 FPGA families
- 6 SERDES chiplets
- 3 Data converter chiplets
- 3 Optical chiplets
- 2 ASIC compute chiplets
- 5 Defense Industrial Base (DIB) partners and chiplets

intel.

Advanced Interface Bus (AIB) Specification

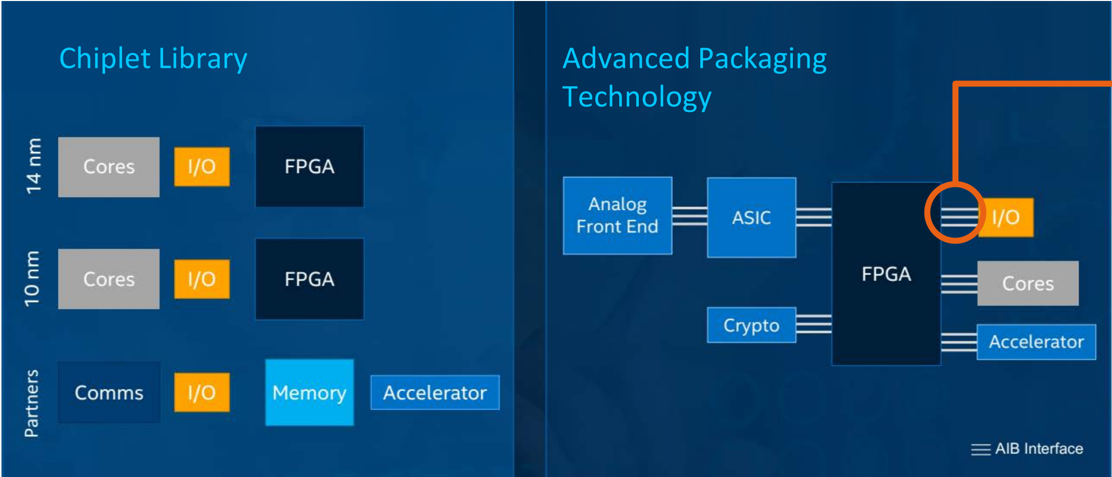
2019.9.18
Revision 1.2

At https://github.com/chipsalliance/aib-phy-hardware

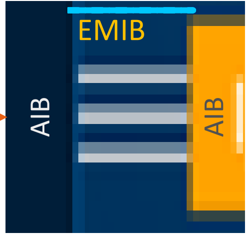


Chiplet Connection with EMIB and AIB

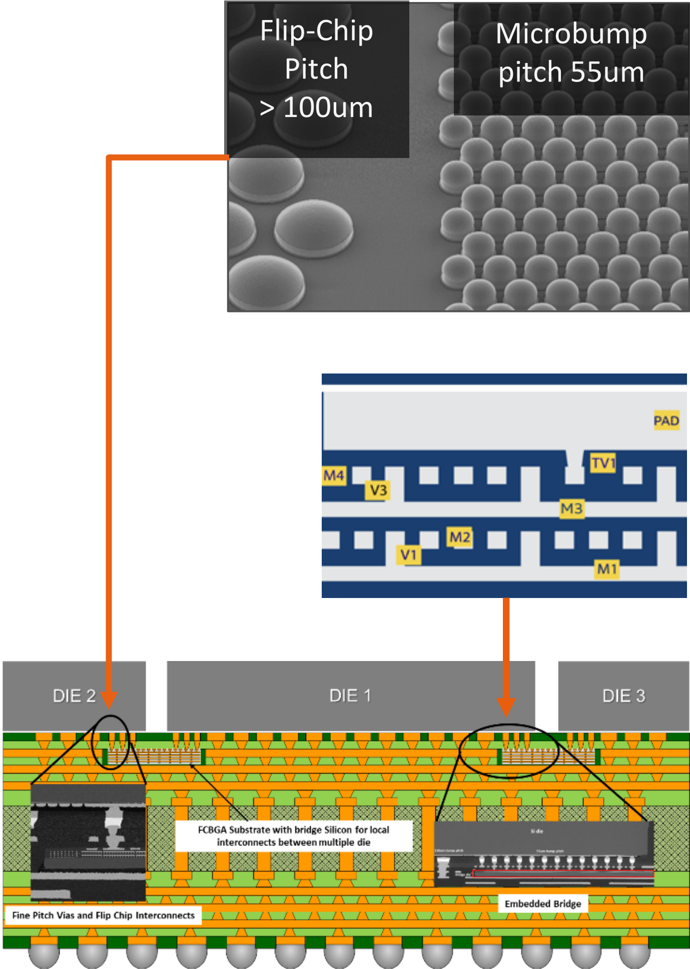
- Platform for innovation through ecosystem
- Explore new business models and technology partnerships



Advanced Interface Bus (AIB)

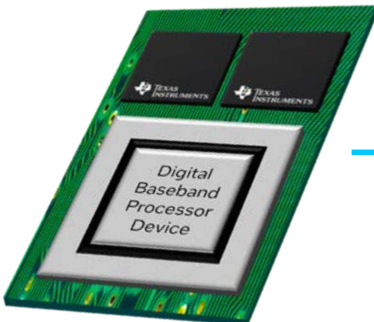


Intel® Embedded Multi-Die Interconnect Bridge (EMIB)

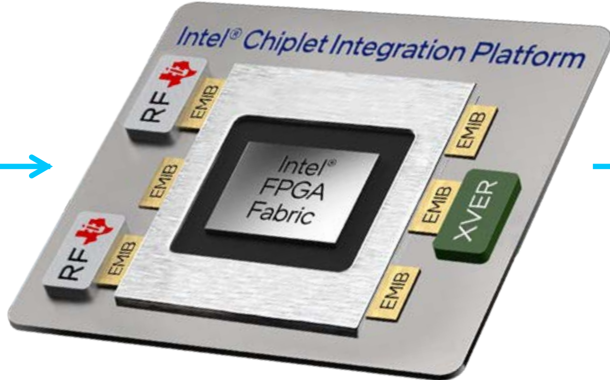


- ADC/DAC
- Machine Learning
- Memory
- Processors
- Adjacent IP
- …Your Ideas

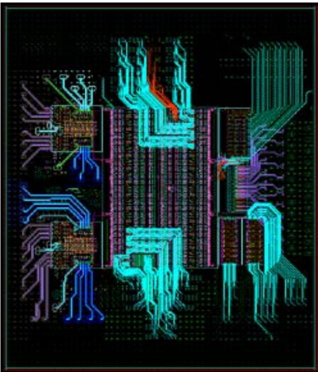
Chiplet Integration



Discrete component platform

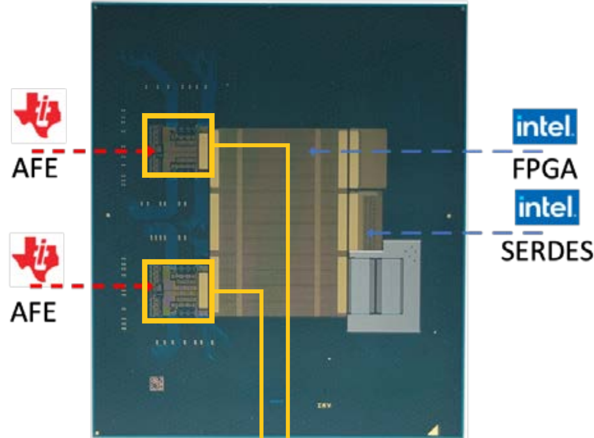


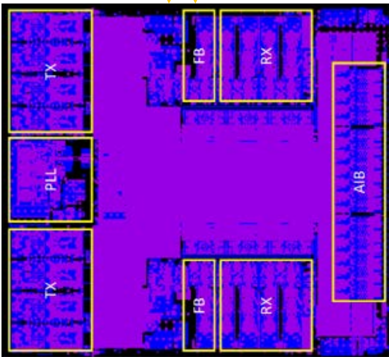
Integrate AFE into FPGA platform



Substrate signal drawing

Substrate physical design





8T8R2AUX AFE floorplan

TI AFE Chiplet Design Features

Configuration: 8T8R2AUX

MAX sample rate:

- DACs: 12GSPS / ADCs: 4GSPS

RF Bandwidth >7 GHz

Digital Features

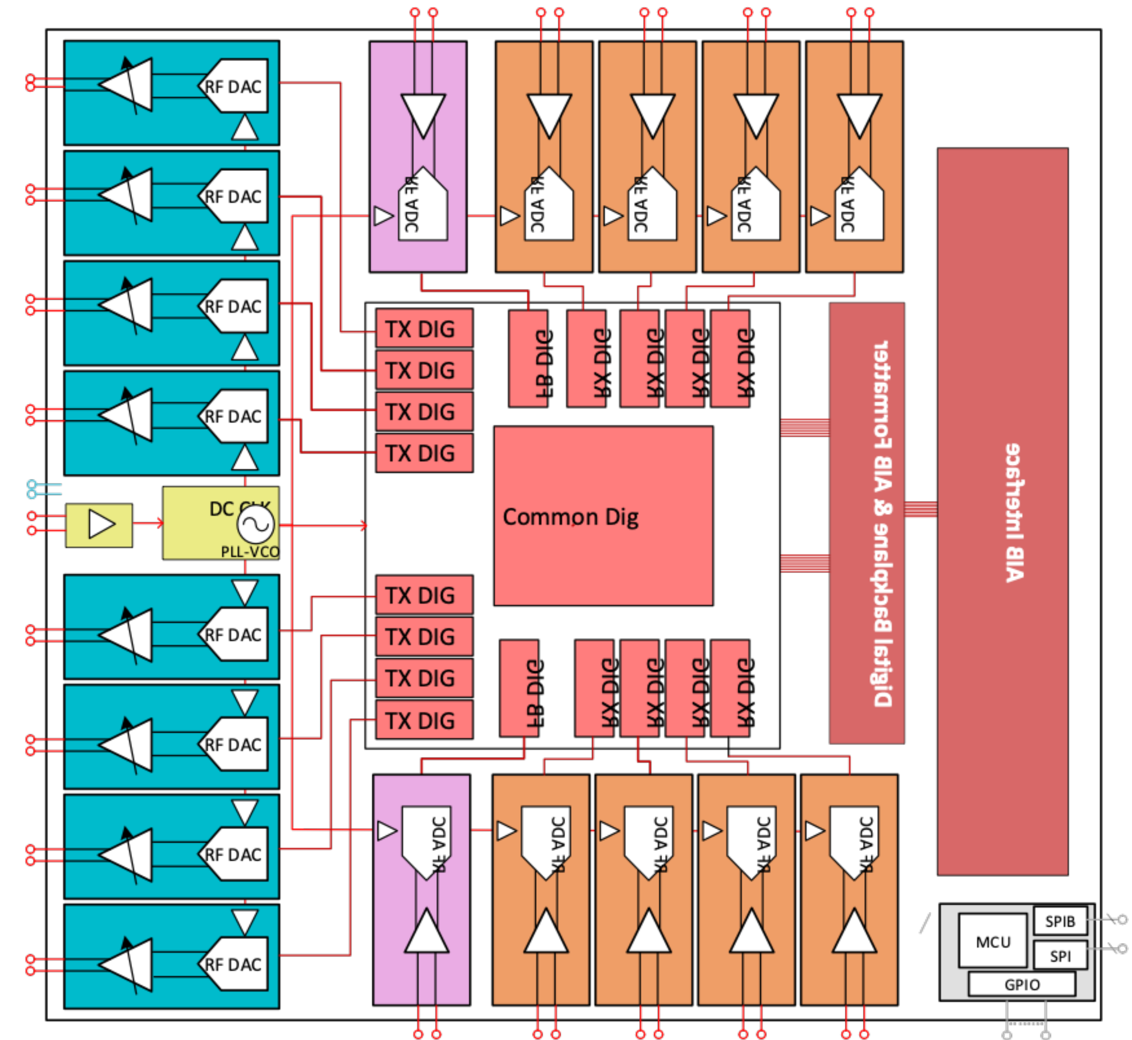
- RX DDC: dual DDC with complex decimation
- AUX DDC: dual DDC with complex decimation
- TX DUC: dual DUC with complex interpolation

Clocking Options:

- internal PLL for TX and RX
- internal PLL for TX and external clock for RX
- external clock for TX and RX

Interface:

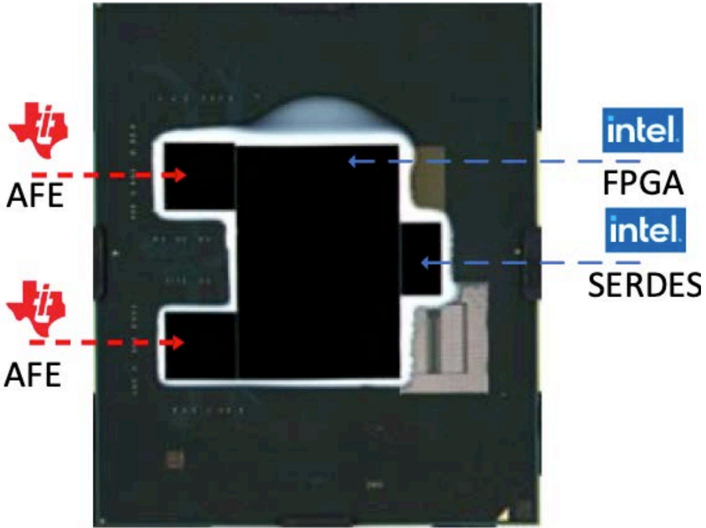
- Die to Die: 16 AIB channels, 16b TX/16b RX, 2Gbps



See datasheet for workloads and configurations. Results may vary.

Heterogeneous Integration Advantages

Chiplet Integration Platform

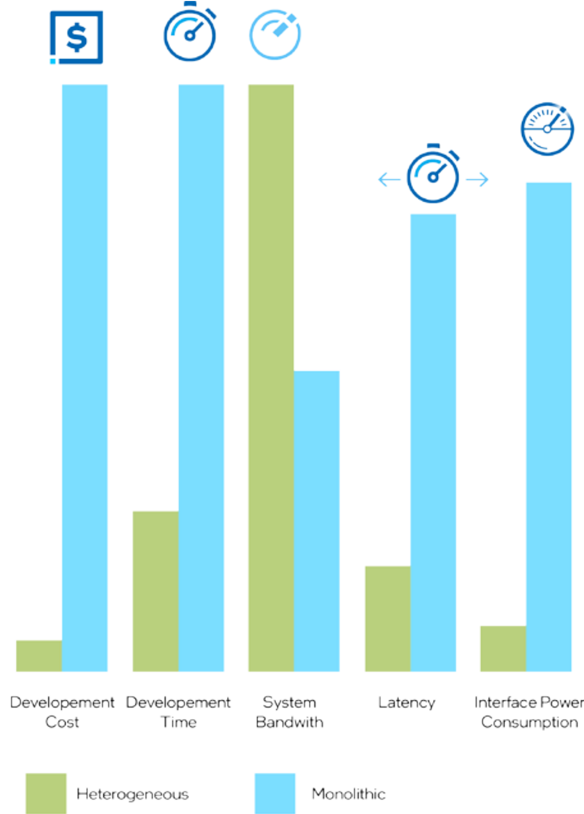


Characterization platform

Results

A. 4 chiplets on 3 process nodes from 2 foundries
B. AIB-enabled Analog Front End (AFE) chiplet from Texas Instruments
C. AIB 1.0 IP with 55µm microbumps

Integration advantages



CHIPS Phase 2 Platform Hardware Overview

Board Management Controller

OCP OpenBMC Formfactor

Power Sequencing (PMBus)

FPGA Configuration

Telemetry (P,I,V,T)

I2C/SPI Controller

UART/Ethernet/USB/JTAG

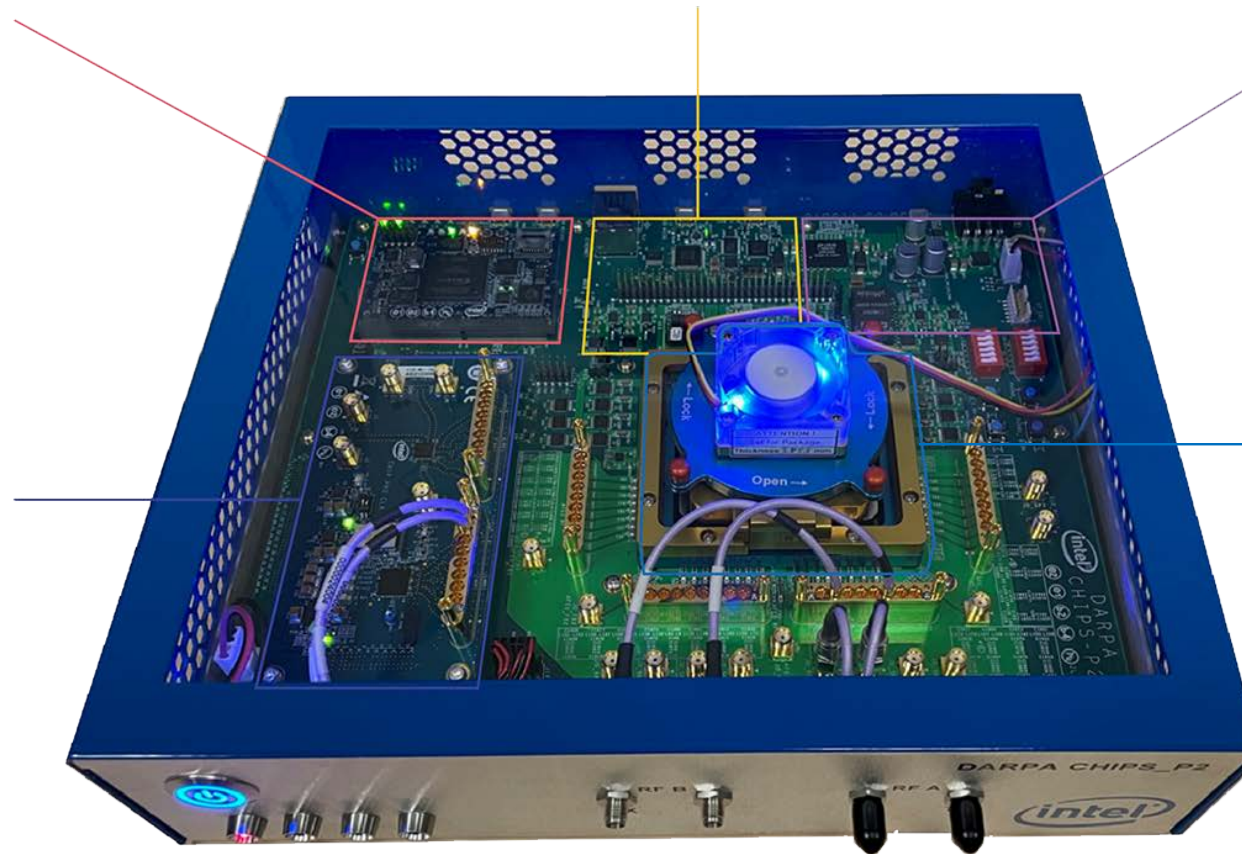
QSPI Flash

Communication Ports

- Ethernet
- USB 2.0 High Speed

Power Supply Network

- In-Rush Current Controller
- FPGA Supplies
- AFE Supplies



RF Clock Board

Clock Gen and Sync

TI LMK04828 (Low Noise PLL)

Low noise LDO

CHIPS P2 Multi-Chip Package

- FPGA fabric die
- 1x 56G XVER
- 2x TI AFE

RF Frontend

- Passive Matching Network
- BALUN
- RF Connectors/Cables

CHIPS Phase 2 Platform Hardware Overview

Board Management Controller

OCP OpenBMC Formfactor

Power Sequencing (PMBus)

FPGA Configuration

Telemetry (P,I,V,T)

I2C/SPI Controller

UART/Ethernet/USB/JTAG

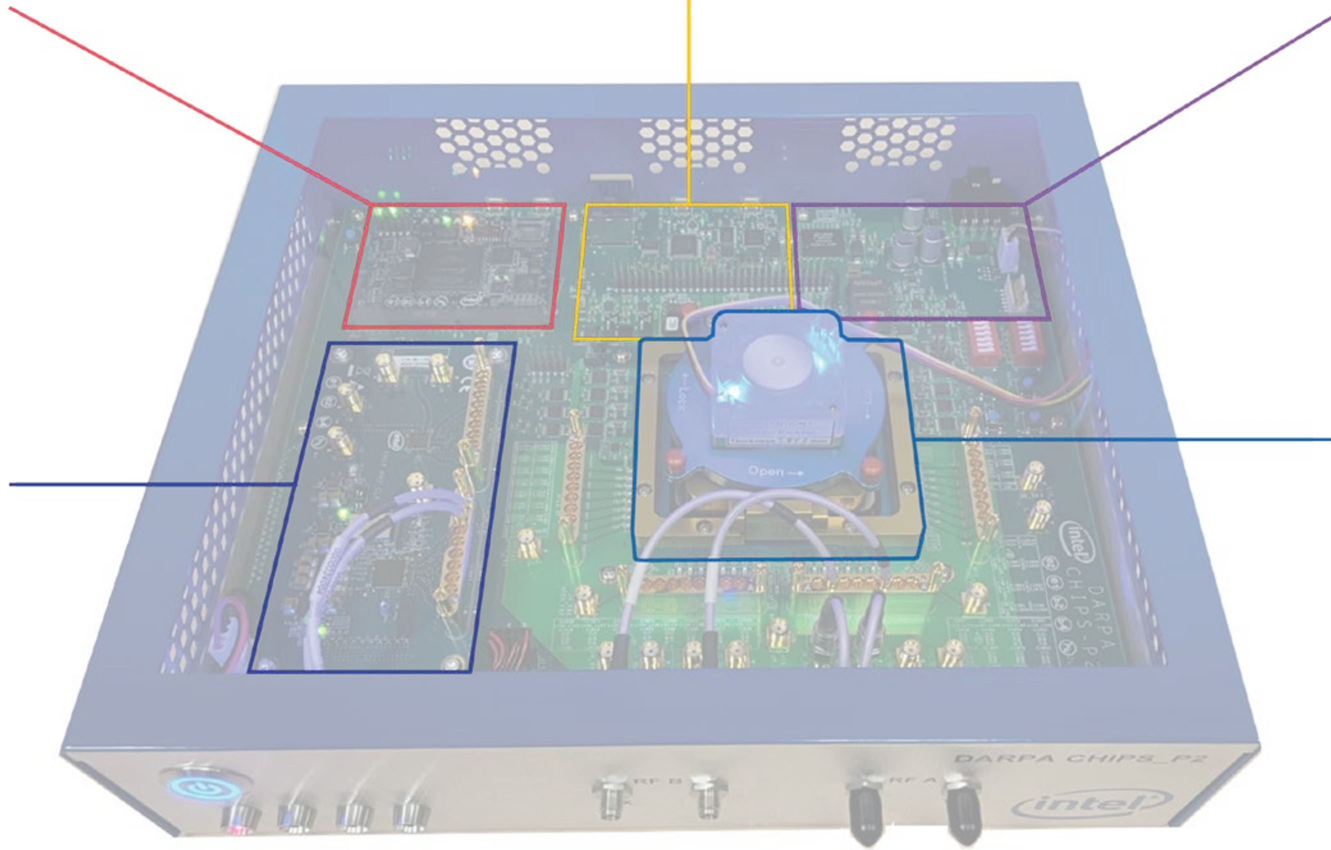
QSPI Flash

Communication Ports

- Ethernet
- USB 2.0 High Speed

Power Supply Network

- In-Rush Current Controller
- FPGA Supplies
- AFE Supplies



RF Clock Board

Clock Gen and Sync

TI LMK04828 (Low Noise PLL)

Low noise LDO

CHIPS P2 Multi-Chip Package

- FPGA fabric die
- 1x 56G XVER
- 2x TI AFE

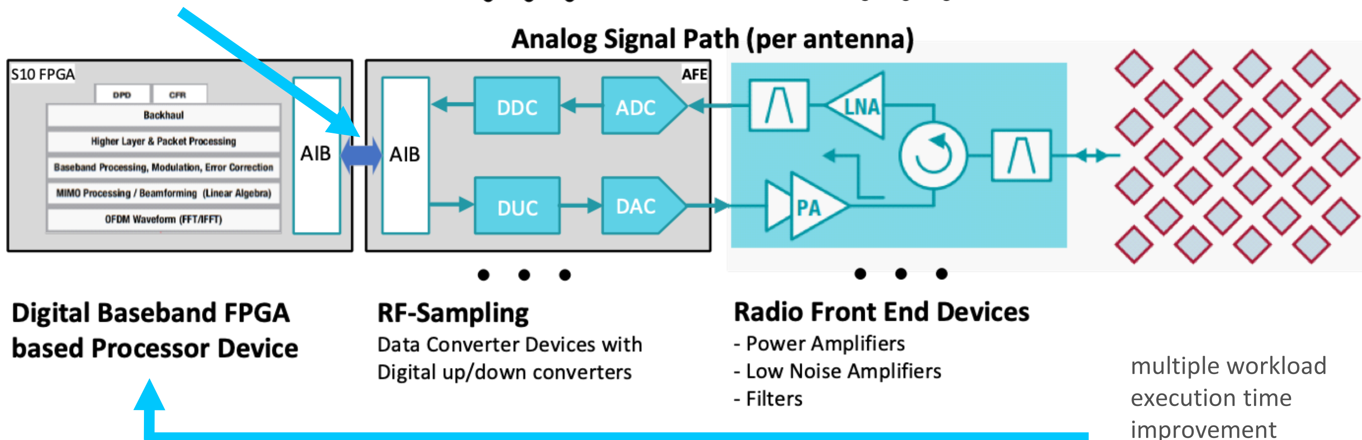
RF Frontend

- Passive Matching Network
- BALUN
- RF Connectors/Cables

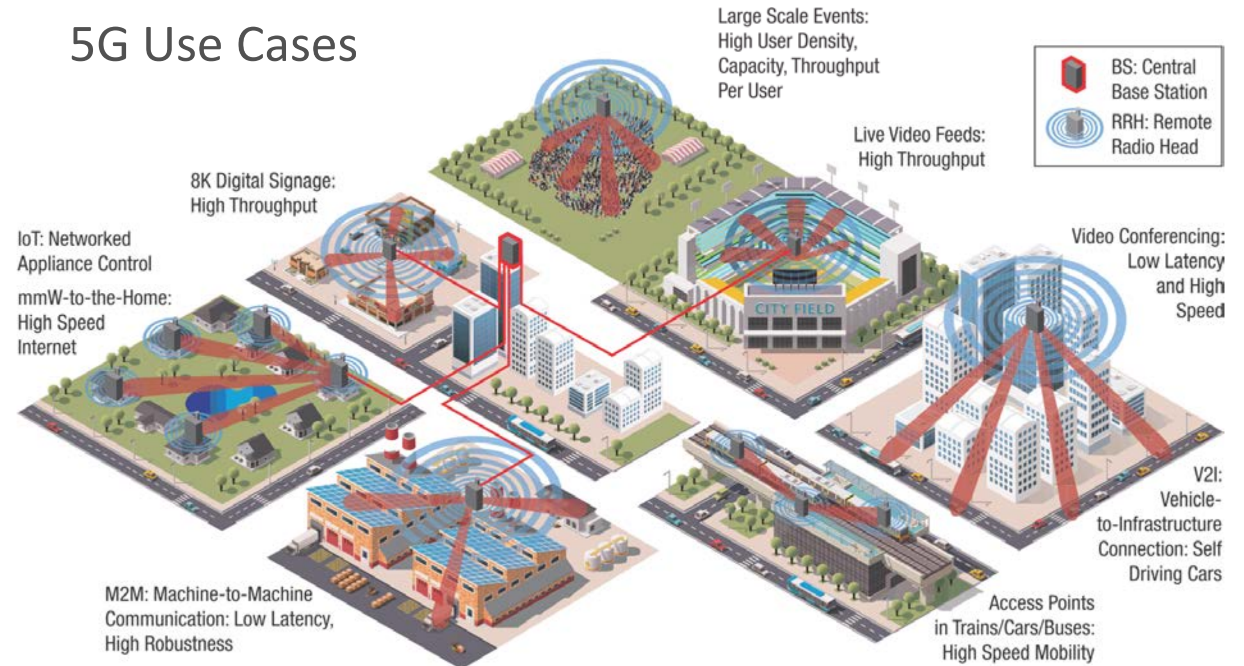
Enabling Massive MIMO

Diagram of proposed base station with FPGA HW acceleration

2x Bandwidth@10x in interface reduction power



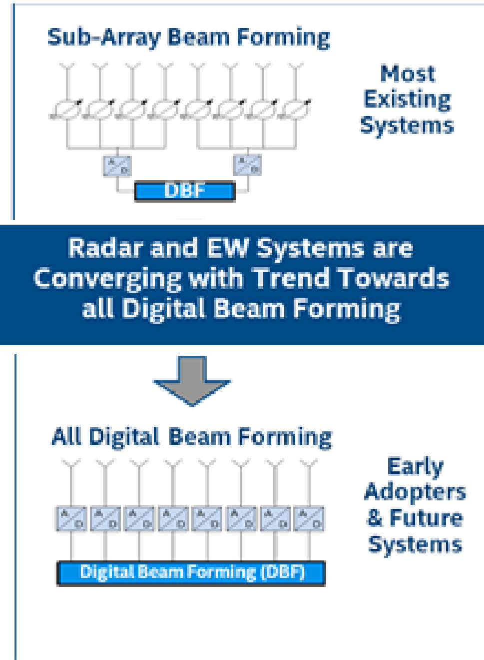
multiple workload execution time improvement

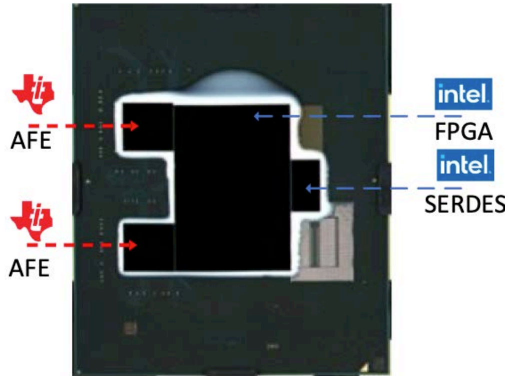


	JESD 204B	AIB
BW	308Gbps	256 Gbps
Channels	26 @ 12.5Gbsp	16 AIB Ch x 2Gbps
Power	25W	0.512W
Latency	135 Frame Clk	6 Frame Clk
Board Complexity	High	Low

Enabling Radar Systems

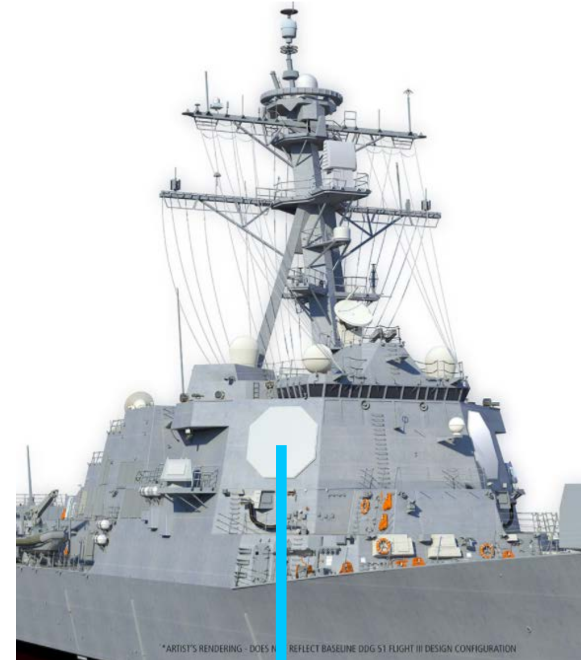
FPGA increases Digital Beamforming Capabilities





8T8R2AUX TI Chiplet

- DACs: 12GSPS
- ADCs: 4GSPS



Air and Missile Defense Radar (AMDR) **upgrade** to US Navy ships with increased search volume in the same amount of search time

Examples of other applications

Lower Tier Air and Missile Defense Radar (LTAMDS)

Enterprise Air Surveillance Radar

Multi Chip Package from CHIPS Phase 2 enables next gen Radar and 5G Comm System

CHIPS Technology Enables Next Generation Systems

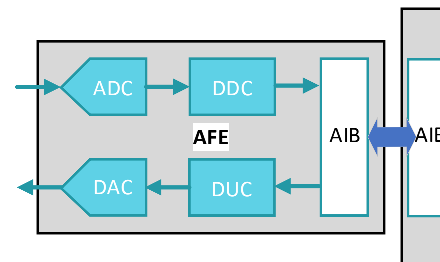
RF Transmitter:

- 12GSPS DAC
- Interpolation x16 at DUC
- Carrier Frequency at 3.5Ghz
- NCO data from FPGA to DUC via AIB

RF Receiver:

- 4GSPS ADC
- Decimation x4 at DDC
- Nyquist Zone Sampling
- Data is forwarded to FPGA via AIB for FFT calculation

CHIPS technology in partnership with Texas Instruments' AFE technology enables next generation RF systems, e.g. in our demonstration by combining AI and full FPGA HW/SW stack, we created a powerful modulation classification capability



Conclusion

Intel and Texas Instruments have successfully developed CHIPS Phase 2 fully functional state-of-the-art MCP.

Breath of technology coverage spans from commercial to military, aerospace and government markets.

We achieved program's objectives of creating and integrating complex heterogeneous system at a fraction of development time and cost without compromising performance.

- Increased bandwidth improvement
- Reduction of interface power
- Ease of board design constraints
- Improved system performance/latency
- Reduced system SWAP

Intel at Hot Chips

Ready to win?

Visit bit.ly/HotWings22 and match Intel speakers to their talks for a chance to win an Intel® NUC Mini PC and other prizes.

Notices & Disclaimers

Intel technologies may require enabled hardware, software or service activation.

No product or component can be absolutely secure.

Your costs and results may vary.

© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.

intel®